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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,262	04/21/2004	Toshiyuki Hata	HITA.0543	4839

7590 04/20/2005

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/828,262	HATA ET AL.
	Examiner	Art Unit
	Chris C. Chu	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Preliminary Amendment

1. Applicant's preliminary amendment filed on April 21, 2004 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, claim 3, line 2, "the bump electrode is provided plurally on the electrode surface" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 15, line 22, after "resin" remove [?] and insert --.--.

Appropriate correction is required.

Claim Objections

4. Claim 1 is objected to because of the following informalities:

a. Claim 1, line 10, "exposed to the upper surface" should be --exposed through the upper surface-- or -- exposed out of the upper surface --.

b. Claim 1, line 11, "exposed to the lower surface" should be --exposed through the lower surface-- or -- exposed out of the lower surface --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 – 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(A) In claim 1, lines 2, 3, 6, 7, 13 and 14, it is unclear what the applicant regards as "an **upper surface** and a **lower surface** as **a** surface and a **back surface**". That is, either "upper surface" or "lower surface," includes the back surface. Therefore, the limitation is repeating the same term by using different words in one sentence, hence the claim cannot be understood.

(B) In claim 3, line 2 and claim 5, line 3, it is unclear what the applicant regards as "the bump electrode is provided **plurally** on the electrode surface". That is, the limitation could read as that one bump electrode is formed on the surface of several electrodes on the chip or plural bump electrodes are formed on the surface of the electrodes on the chip. Thus, the claim cannot be understood.

(C) In claim 5, line 4, the term "large" is a relative term which renders the claim indefinite. The term "large" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

(D) In claim 12, line 3, the term "about" is a relative term which renders the claim indefinite. The term "about" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

(E) In claim 13, line 2, it is unclear what the applicant regards as "a transistor is formed on the semiconductor chip". That is, the term "transistor" describes a second chip that stacked on the semiconductor chip or the term "transistor" defines that the semiconductor chip is a transistor. Thus, the claim cannot be understood.

(F) In claim 14, line 2, "the electrode region" lacks antecedent basis. Furthermore, in line 4, the term "near" is a relative term which renders the claim indefinite. The term "near" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

(G) The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a Japanese document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 – 6, 9, 13 and 14, as best understood by the examiner, are rejected under 35 U.S.C. 102(e) as being anticipated by Madrid et al. (U. S. Pat. No. 6,777,800).

Regarding claim 1, Madrid et al. discloses in e.g., Fig. 1 and Fig. 5 a semiconductor device (100; column 3, lines 47 – 48) comprising:

- a sealing member (102; column 3, line 51) formed of an insulating resin (column 3, lines 54 – 55) and having an upper surface and a lower surface as a surface and a back

surface, respectively, and side faces connecting the upper and lower surfaces with each other;

- a semiconductor chip (108; column 3, line 66) positioned within the sealing member, the semiconductor chip including electrodes (pads under the elements 115) respectively on a first main surface (a portion of active surface of the chip 108 that connected to the source lead structure 103) and a second main surface (a portion of active surface of the chip 108 that connected to the gate lead 112) thereof as a surface and a back surface, respectively;
- a first electrode plate (101 and 107; column 4, line 45) having an upper surface and a lower surface as a surface and a back surface, respectively, a part of the upper surface (101(a)) of the first electrode plate being exposed to the upper surface of the sealing member and the lower surface portions of end portions (177 and 107) of the first electrode plate being exposed to the lower surface of the sealing member (see e.g., Fig. 5); and
- a second electrode plate (103 and 171; column 4, lines 54 – 55 and column 4, line 43) having an upper surface and a lower surface as a surface and a back surface, respectively, the lower surface (103(a)) of the second electrode plate being exposed to the lower surface of the sealing member and the upper surface of the second electrode plate being positioned within the sealing member (see e.g., Fig. 5),
- wherein the electrode (pads under the elements 115) on the second main surface of the semiconductor chip is electrically connected to the first or the second electrode plate through an electrically conductive adhesive (see e.g., Fig. 5), and

- wherein a bump electrode (115; column 5, line 29) is formed on a surface of the electrode formed on the first main surface of the semiconductor chip, the bump electrode is covered with an electrically conductive adhesive (114; column 5, line 30), and the bump electrode and the second or the first electrode plate are electrically connected to each other through the adhesive (column 5, lines 29 – 31).

Regarding claim 2, Madrid et al. discloses in e.g., Fig. 1 and Fig. 5 the bump electrode (115) and the second or the first (101 and 107) electrode plate being not in contact with each other (see e.g., Fig. 5).

Regarding claim 3, Madrid et al. discloses in e.g., Fig. 1 and Fig. 5 the bump electrode (115) being provided one or plurally on the electrode surface (at the pads under the elements 115).

Regarding claim 4, Madrid et al. discloses in e.g., Fig. 1 and Fig. 5 the bump electrode (115) being a "stud type" bump electrode formed on the electrode provided on the first main surface of the semiconductor chip.

Regarding claim 5, Madrid et al. discloses in e.g., Fig. 1 and Fig. 5 the bump electrode (115) being a stud type bump electrode formed on the electrode provided on the first main surface of the semiconductor chip, and the bump electrode being provided plurally on the electrode surface, of which the bump electrode(s) having a "large height" is (are) in contact with the first or the second electrode plate and the other bump electrodes (the elements 141 that are connected to the gate lead 112; column 2, lines 49 – 51 and column 4, lines 43 – 45) are not in contact with the first or the second electrode plate (see e.g., Fig. 3).

Regarding claim 6, Madrid et al. discloses in e.g., Fig. 5 a recess (113) being formed in the surface of the first or the second electrode plate in an opposed relation to the bump electrode.

Regarding claim 9, Madrid et al. discloses in e.g., Fig. 5 the first electrode plate (101 and 107) and the second electrode plate (103) extending in different directions.

Regarding claim 13, Madrid et al. discloses in e.g., Fig. 5 and column 3, line 66 – column 4, line 17

- wherein a transistor (VDMOS transistor that formed on the upper surface of the semiconductor die 108; column 4, lines 1 – 17) is formed on the semiconductor chip (108), and a second electrode (the pads on the chip and connected to the gate region of the transistor) of the transistor is formed on the second main surface of the semiconductor chip,
- wherein a "first" electrode and a "control" electrode (any two pads that are formed on the die 108 and connected to the source region of the transistor. Furthermore, since the terms "first" and "control" are intended use of the claimed electrodes that does not differentiate the claimed electrodes over Madrid et al.) of the transistor are formed on the first main surface of the semiconductor chip,
- wherein the first or the second electrode plate (103 and 171) is provided plurally, the second electrode is connected to the second or the first electrode plate (see Fig. 5 and column 4, lines 43 – 45), and
- wherein the first electrode and the control electrode are connected separately to the plural first or second electrode plates (see Fig. 5).

Regarding claim 14, Madrid et al. discloses in e.g., Fig. 5 the adhesive (114; column 5, lines 30 – 31) which covers the bump electrode (115) is spread over both the electrode region (103 and 171) in which the bump electrode is formed and a region deviated from the electrode region and reaching positions near ends of the semiconductor chip (see the elements 114 that spread to near the left and right ends of the chip 108).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7, 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madrid et al. in view of Lam et al. (U. S. Pat. No. 6,256,200).

Regarding claims 7 and 8, while Madrid et al. teaches the use of the electrode plates, Madrid et al. does not appear to provide the ends of the electrode plates being each branched to plural branch ends which project to the outside from the side faces of the sealing member. Lam et al. teaches in e.g., Fig. 8F the ends of electrode plates (148A, 148B in e.g., Fig. 8F and 144A in e.g., Fig. 10C) being each branched to plural branch ends (column 9, lines 8 and 13 – 16) which project to the outside from the side faces of a sealing member (156; see Fig. 8F and Fig. 10C). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to change the ends of the electrode plates to be projected to the outside from

the side faces of a sealing member of Madrid et al. as taught by Lam et al. to form a surface mount package (column 9, lines 16 – 17).

Regarding claim 15, Madrid et al. teaches the sealing member (102) being in a quadrangular shape having four of side faces (see e.g., Fig. 1). However, Madrid et al. does not teach ends of a first electrode plate project from a pair of opposed side faces of the sealing member, and ends of a second electrode plate project from the other pair of side faces intersecting said pair of opposed side faces of the sealing member. Lam et al. teaches in e.g., Fig. 8F the ends of first and second electrode plates (148A, 148B in e.g., Fig. 8F and 144A in e.g., Fig. 10C) projecting from the side faces of the sealing member (156; see Fig. 8F and Fig. 10C). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to change the ends of the electrode plates to be projected to the outside from the side faces of a sealing member of Madrid et al. as taught by Lam et al. to form a surface mount package (column 9, lines 16 – 17).

Furthermore, a further difference between the claimed invention and Madrid et al. and Lam et al., is the location of the projected ends of first and second electrode plates. It would have been obvious to one having ordinary skill in the art at the time the invention was made to rearrange the ends of a first electrode plate formed a pair of opposed side faces of the sealing member and the ends of a second electrode plate formed at the other pair of side faces intersecting said pair of opposed side faces of the sealing member, since it has been held that rearranging parts of an invention involves only routine skill in the art and motivate to do so because these were conventional arrangement used for these respective structures. In re Japikse, 86 USPQ 70.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madrid et al. in view of Hirashima et al. (U. S. Pat. No. 6,479,888).

While Madrid et al. teaches the use of the electrode, Madrid et al. does not appear to provide any example of the electrode's specific composition. Hirashima et al. teaches in Fig. 1(b) and column 8, lines 17 – 19 electrode (21) is composed of an aluminum film. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the aluminum film as the specific material to form the electrode material on the semiconductor die of Madrid et al. as taught by Hirashima et al. to provide excellent resistance to corrosion in many environments.

12. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madrid et al. in view of Maeno et al. (U. S. Pat. No. 6,222,738).

While Madrid et al. teaches the use of the bump electrode and the adhesive, Madrid et al. does not appear to provide any example of the electrode's and adhesive's specific compositions. Maeno et al. teaches in Fig. 1(a) - Fig. 2(h) bump electrode (21) is composed of a gold wire (column 5, lines 33 – 46) and adhesive (8 and 11) is composed of silver paste (column 6, lines 38 – 39) having been cured (column 7, lines 22 – 24). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the gold and silver paste as the specific material to form the bump electrode and adhesive materials on the semiconductor die of Madrid et al. as taught by Maeno et al. to reduce the connection resistance (column 7, lines 9 – 12).

13. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Madrid et al. in view of Shigeno et al. (U. S. Pat. No. 6,372,625).

While Madrid et al. teaches the space between the chip and the electrode plate, Madrid et al. does not appear to provide any example of the thickness of the space. Shigeno et al. teaches in Fig. 2 a space between a chip and electrode plate being about 30 μm (column 3, lines 62 – 65). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the thickness of the space between the semiconductor die and the electrode plate of Madrid et al. as taught by Shigeno et al. to provide a thin semiconductor device (column 1, lines 57 – 58).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Moriguchi, Sakamoto et al., Glenn et al., Fillion et al. and Kinzer disclose a transistor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, April 14, 2005

GEORGE ECKERT
PRIMARY EXAMINER